

FIG. 1

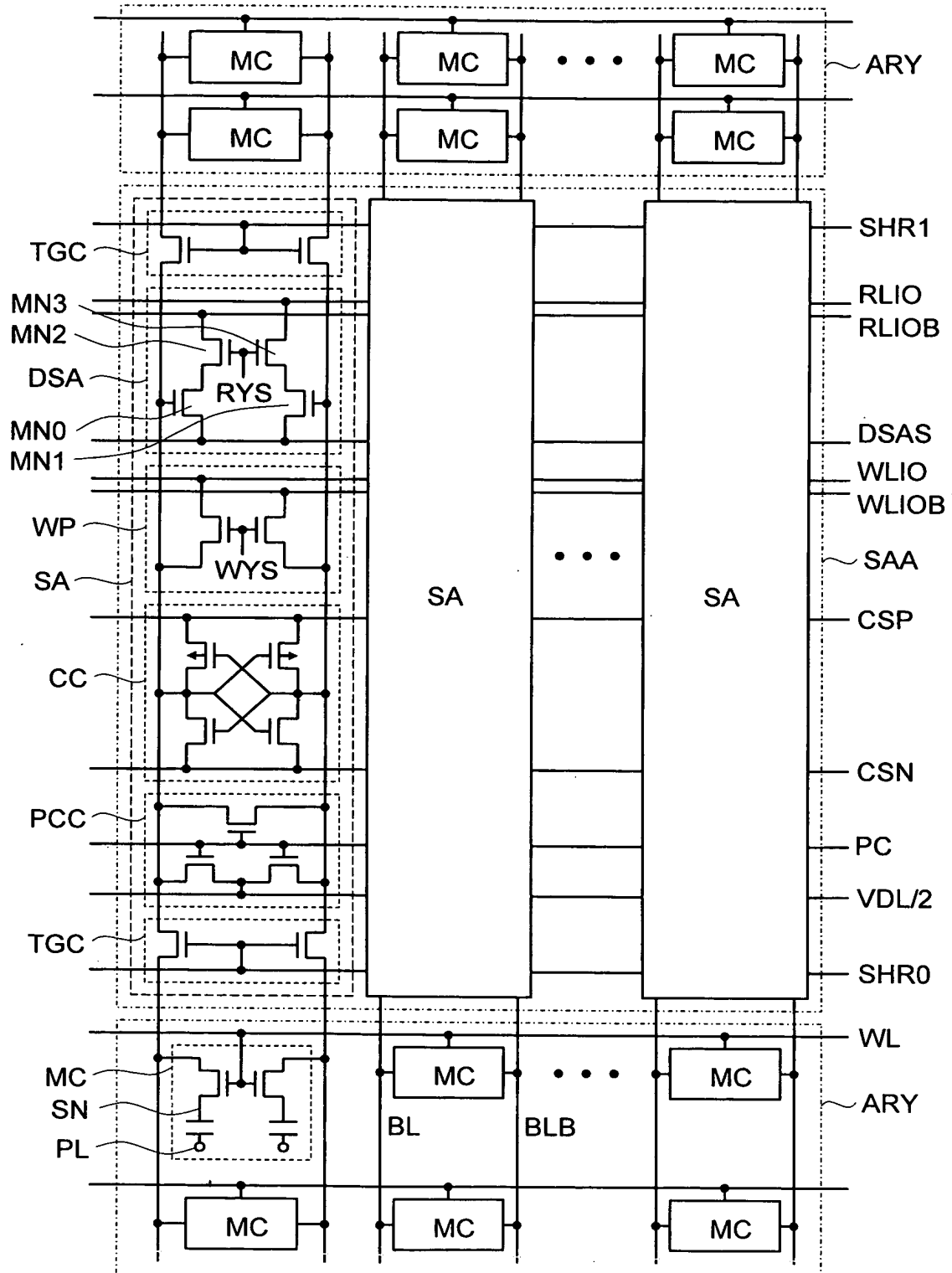


FIG. 2A

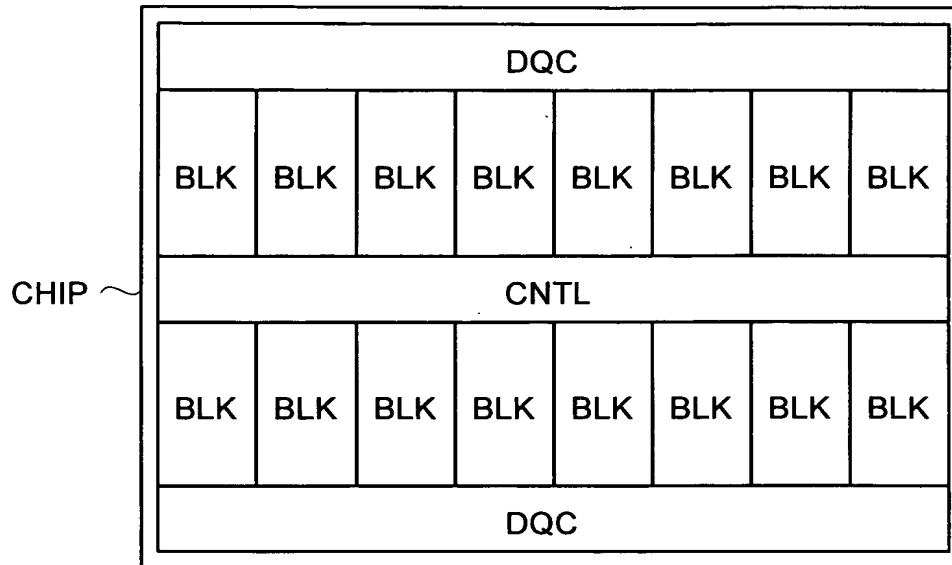


FIG. 2B

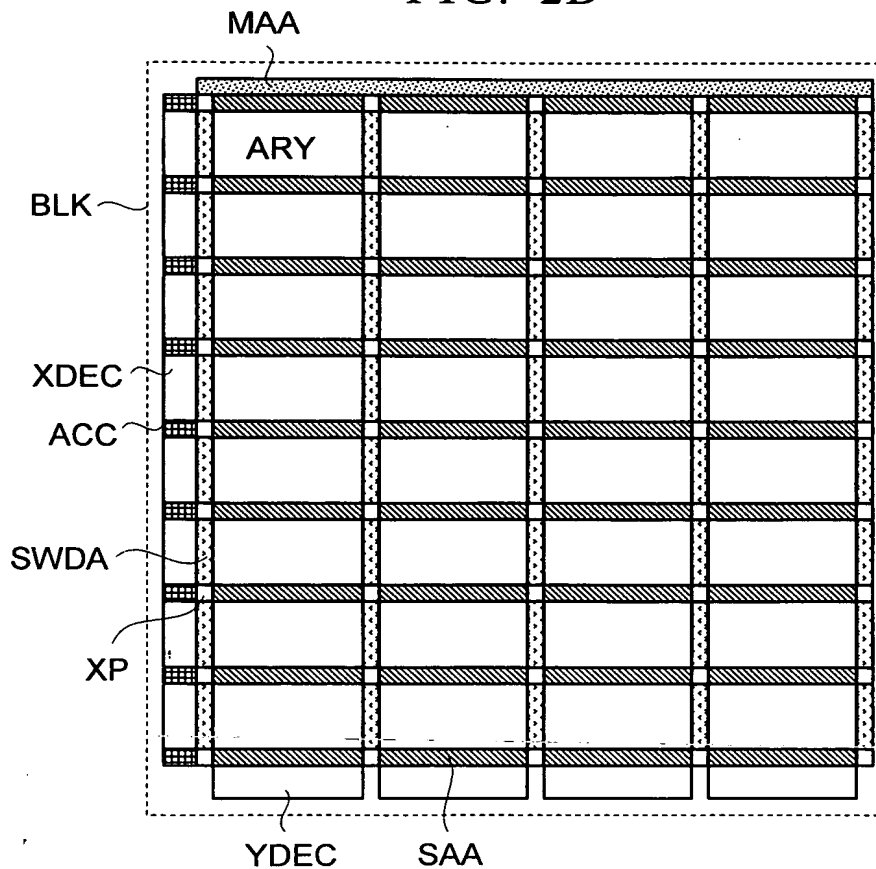


FIG. 3A

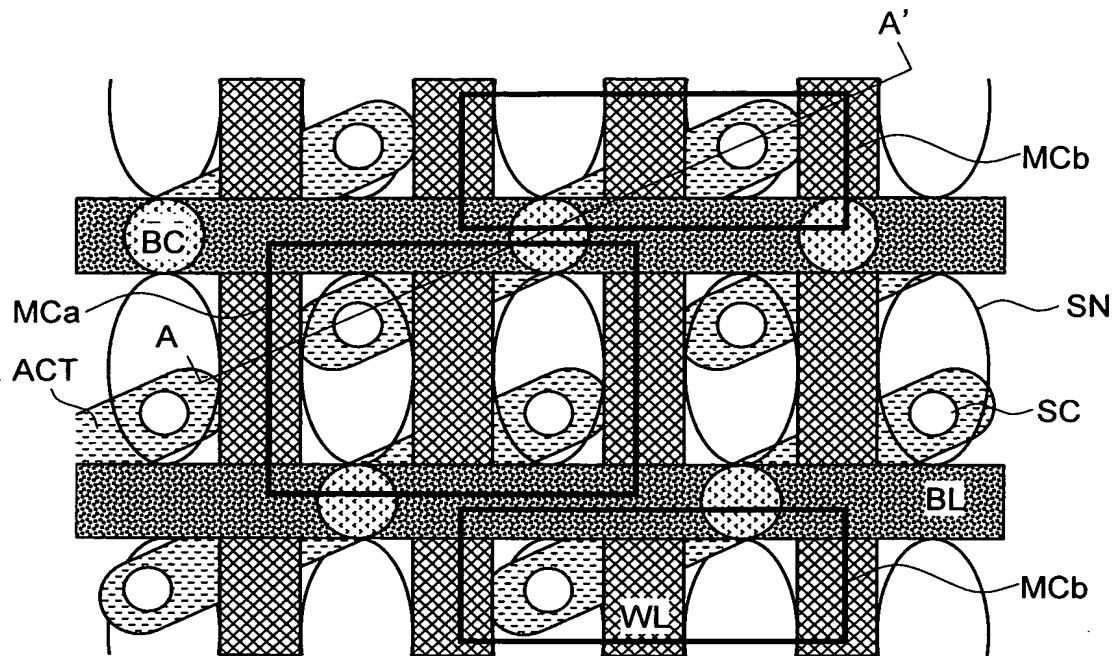
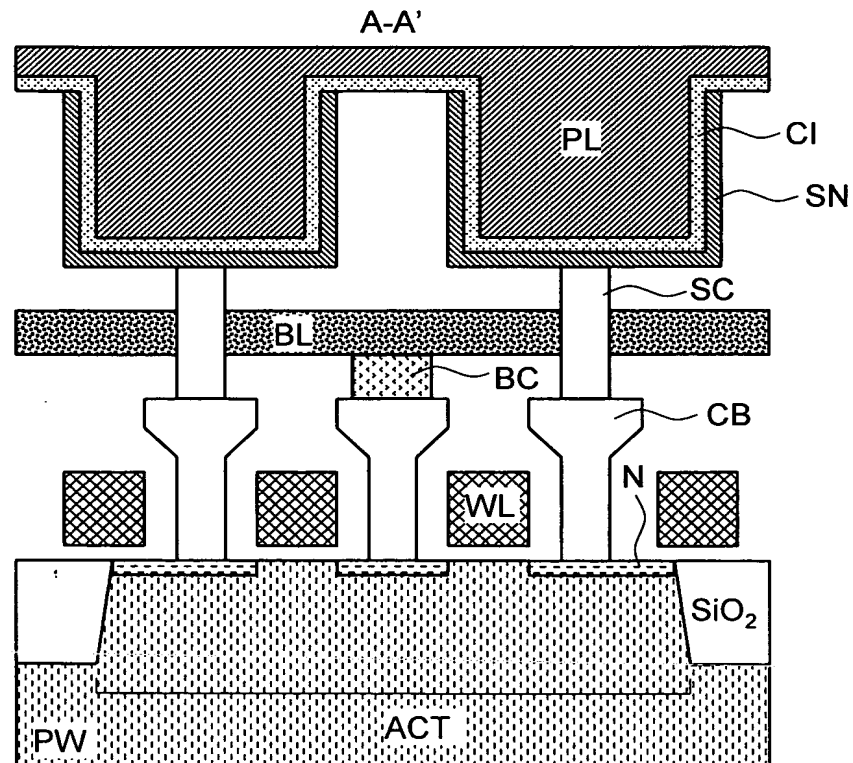


FIG. 3B



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FIG. 4

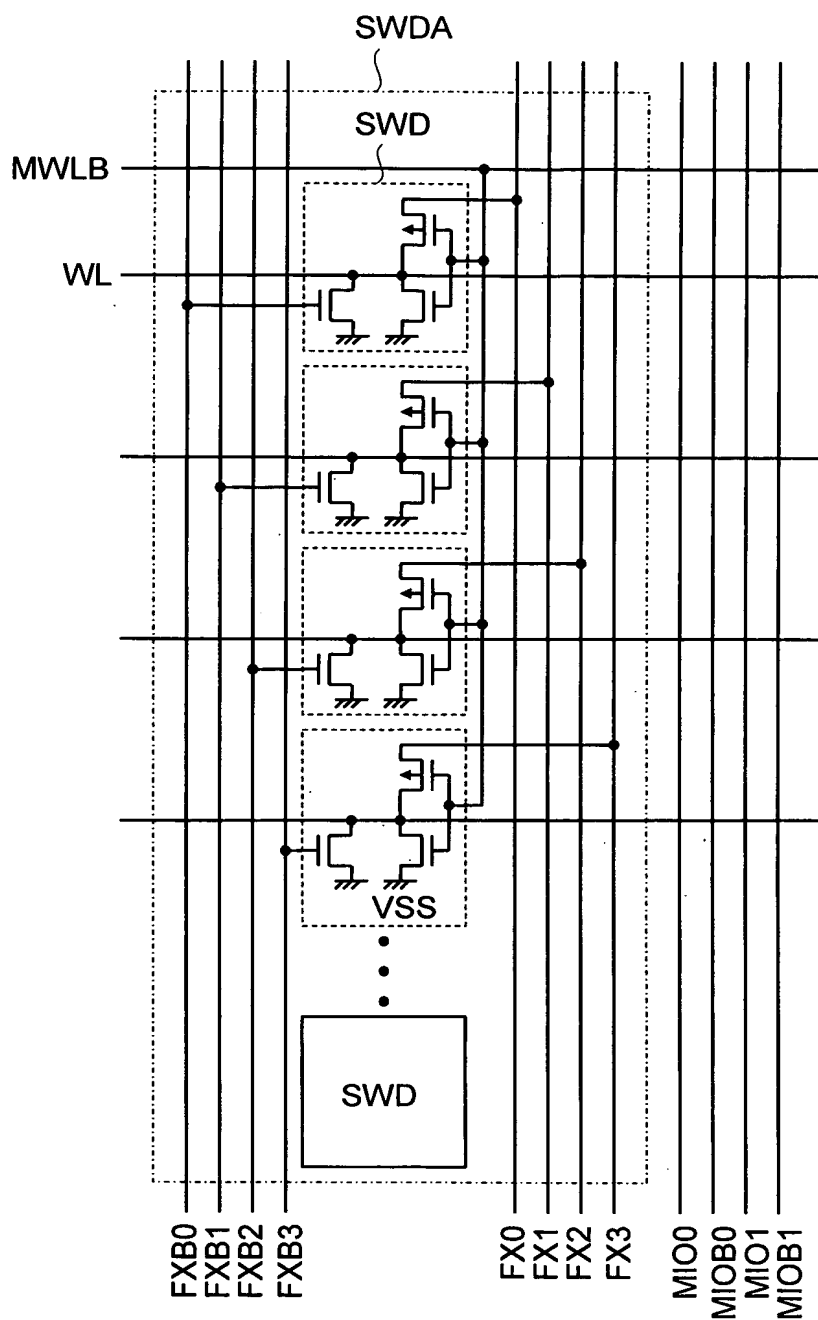


FIG. 5

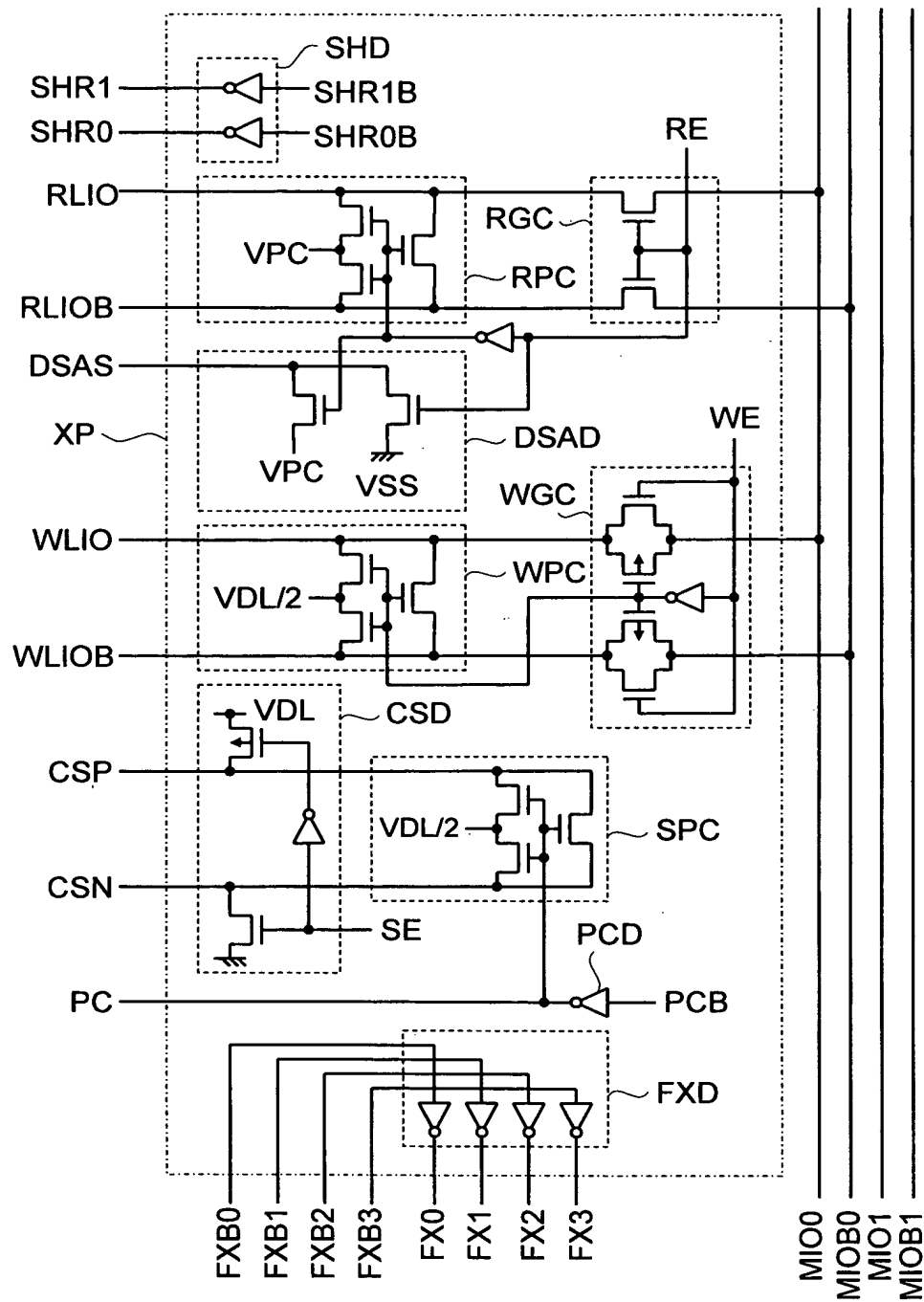
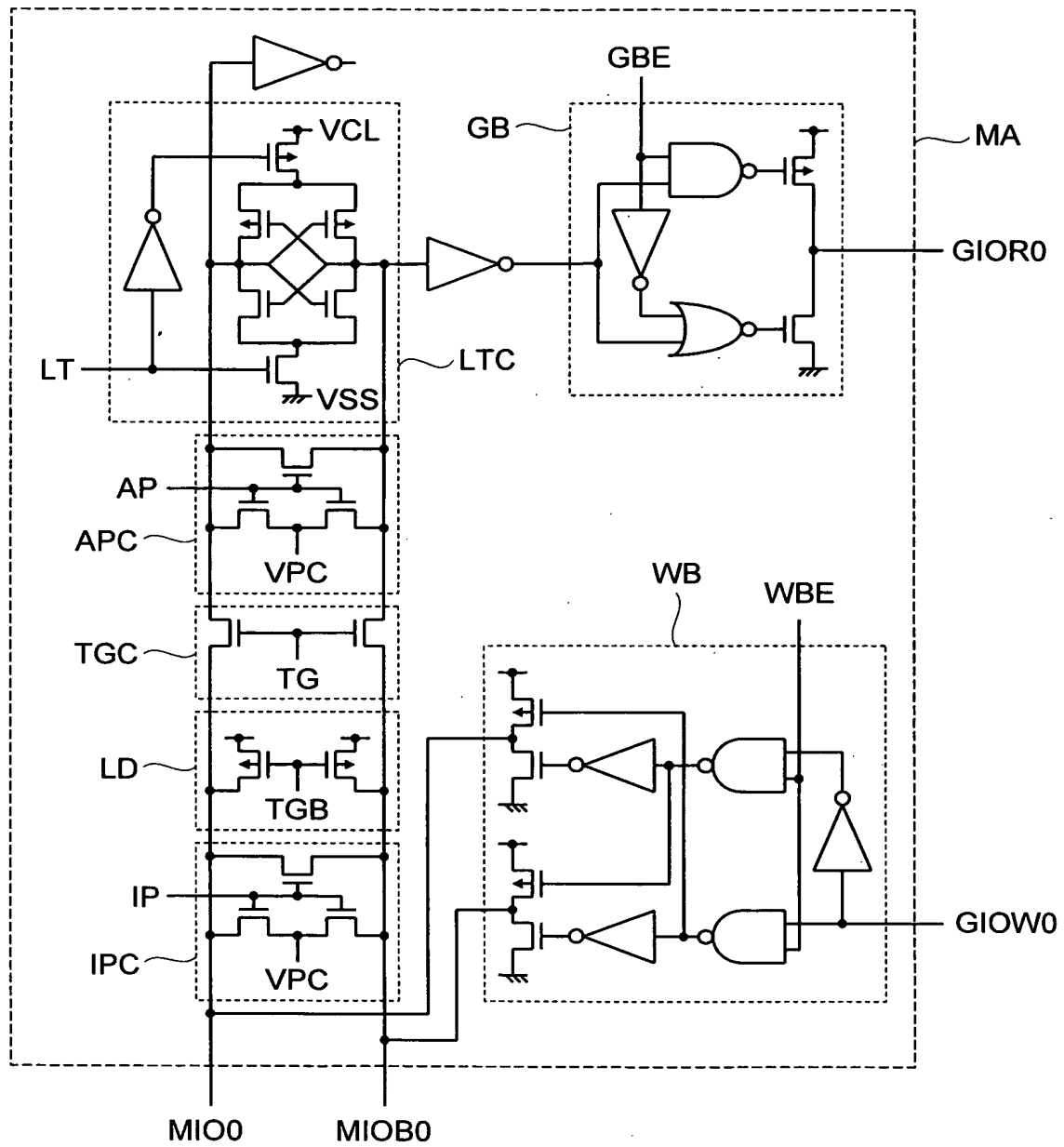
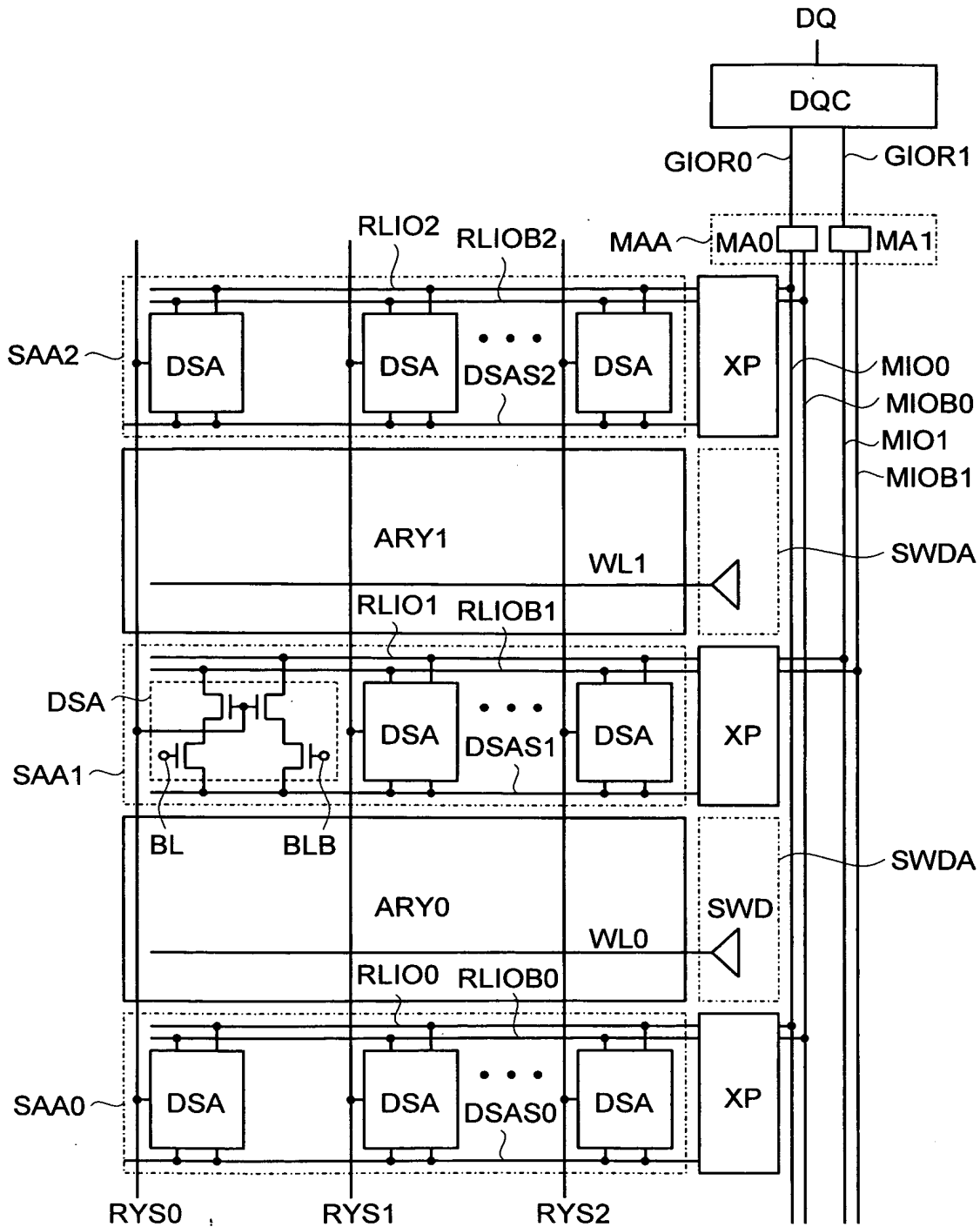


FIG. 6



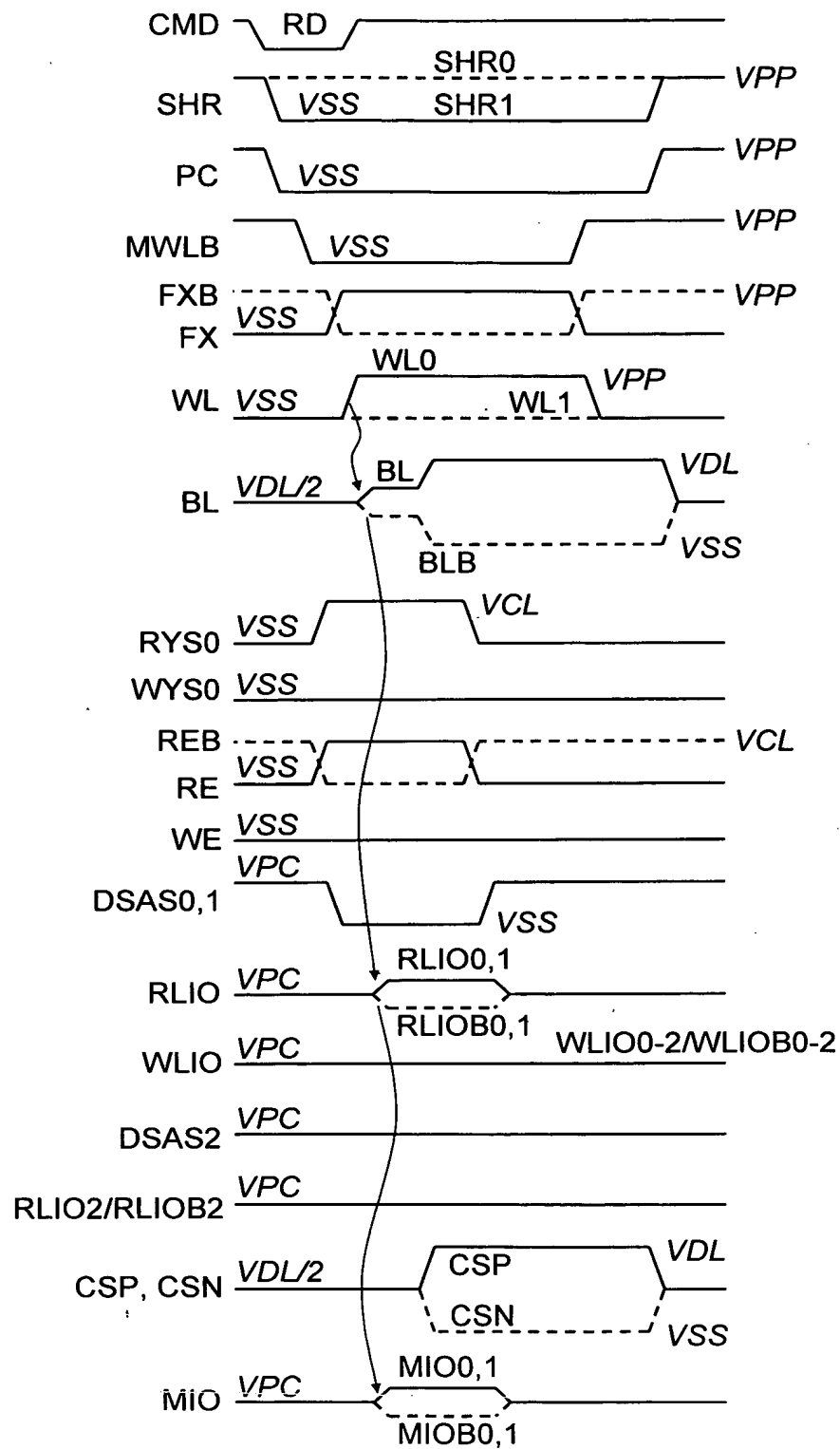
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FIG. 7



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FIG. 8





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FIG. 9

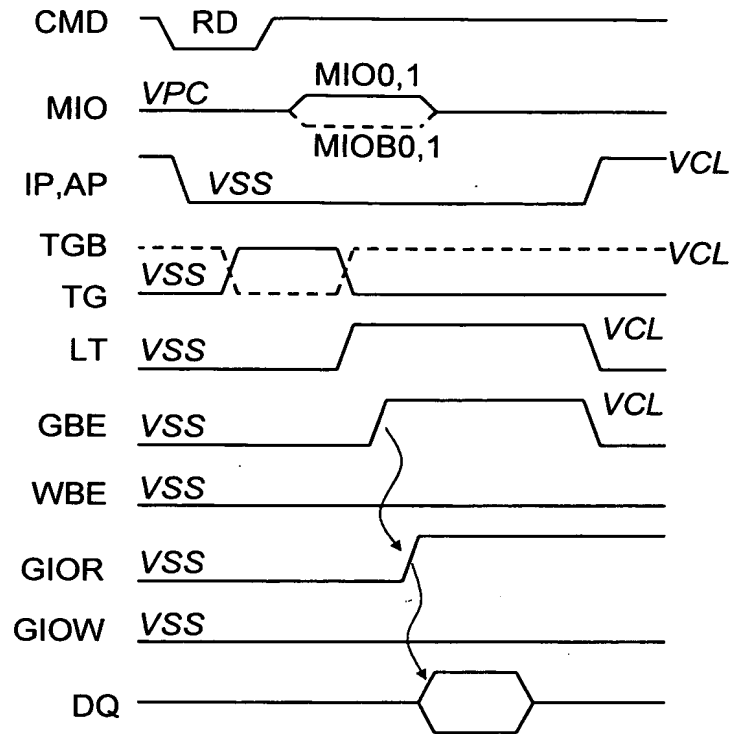
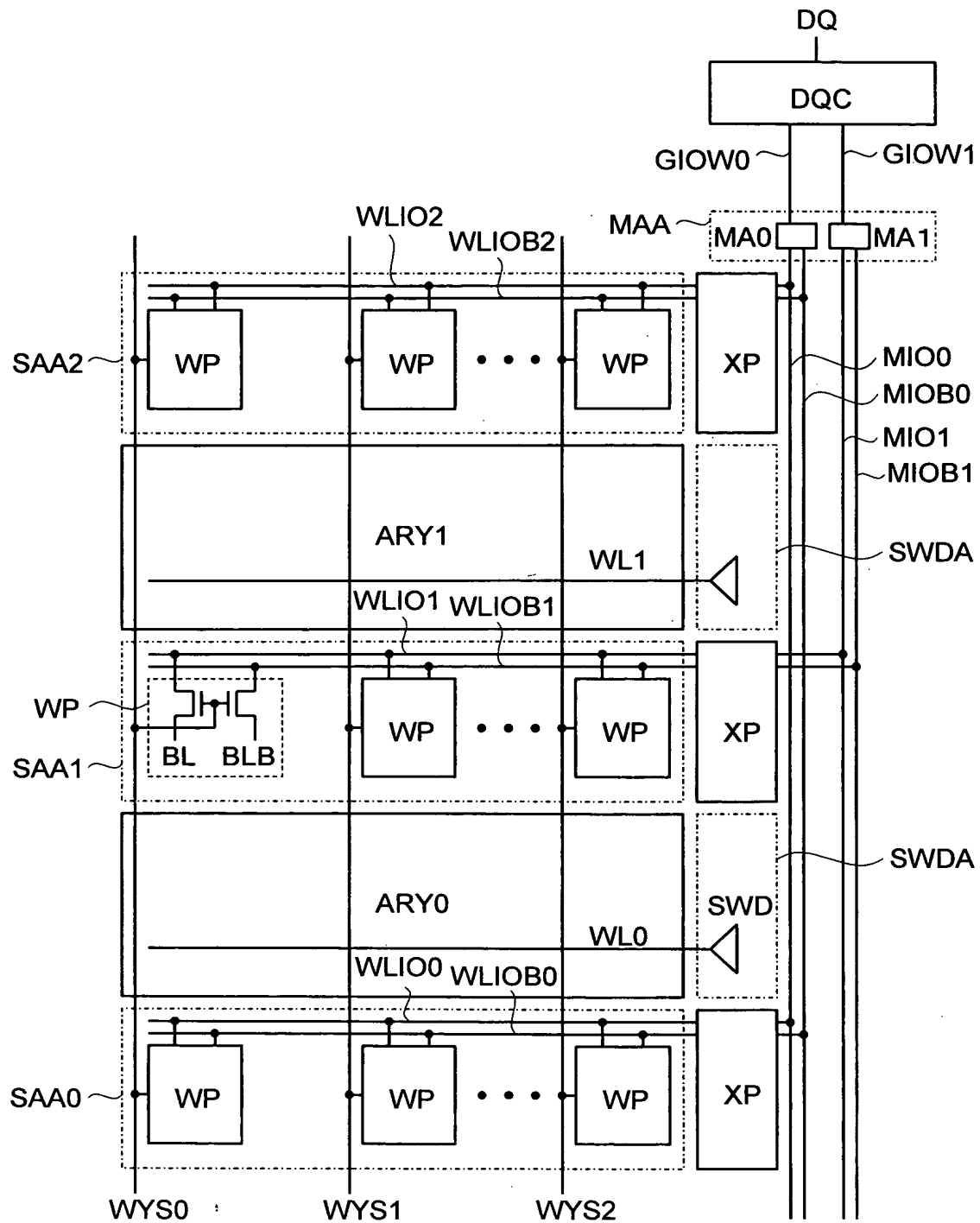
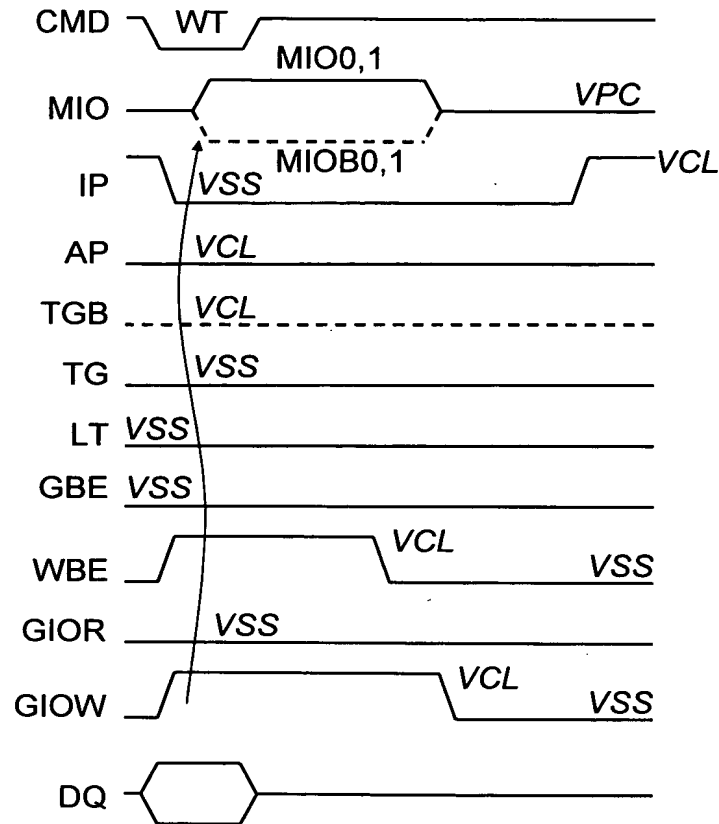


FIG. 10



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FIG. 11



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FIG. 12

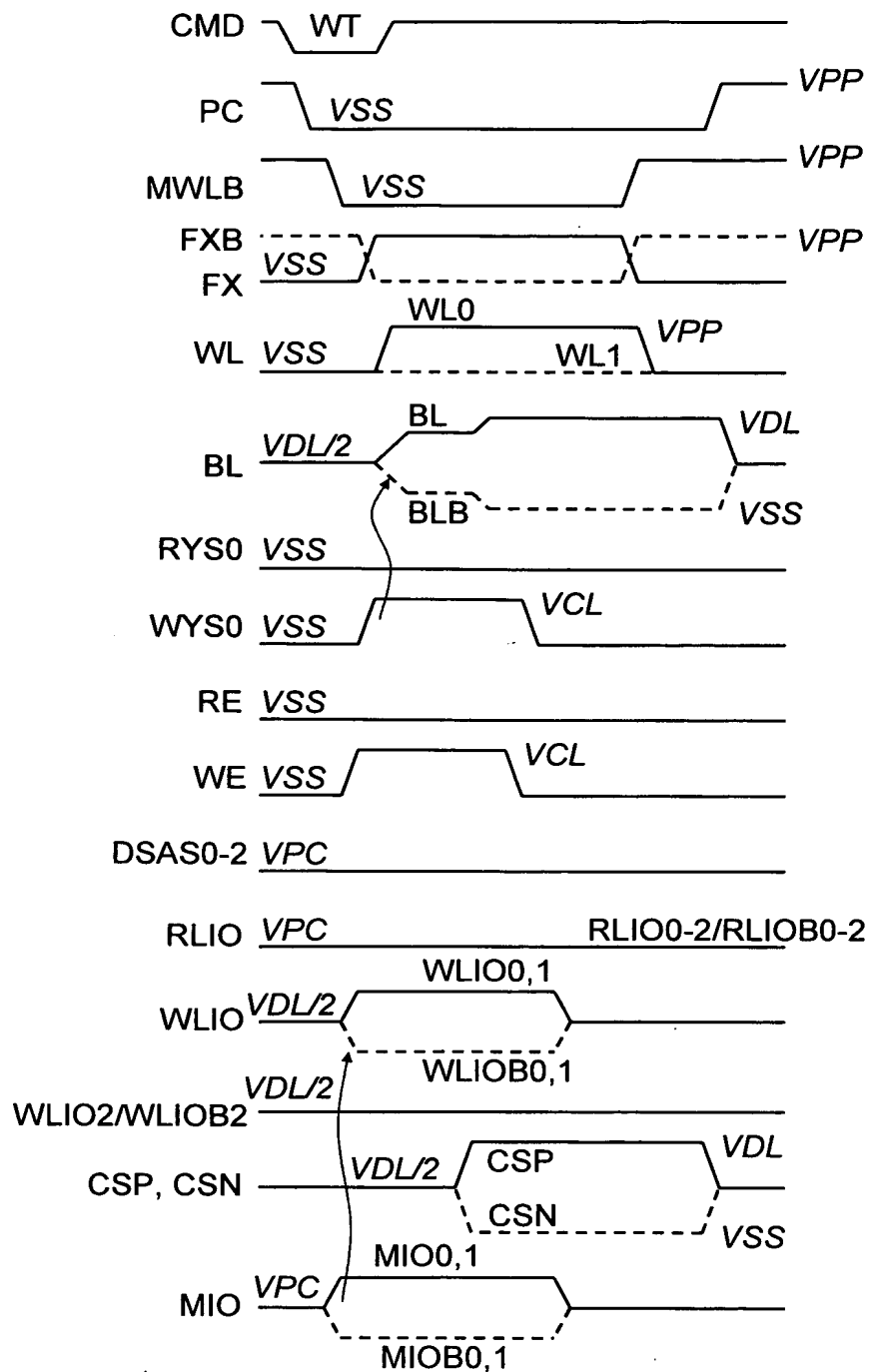


FIG. 13

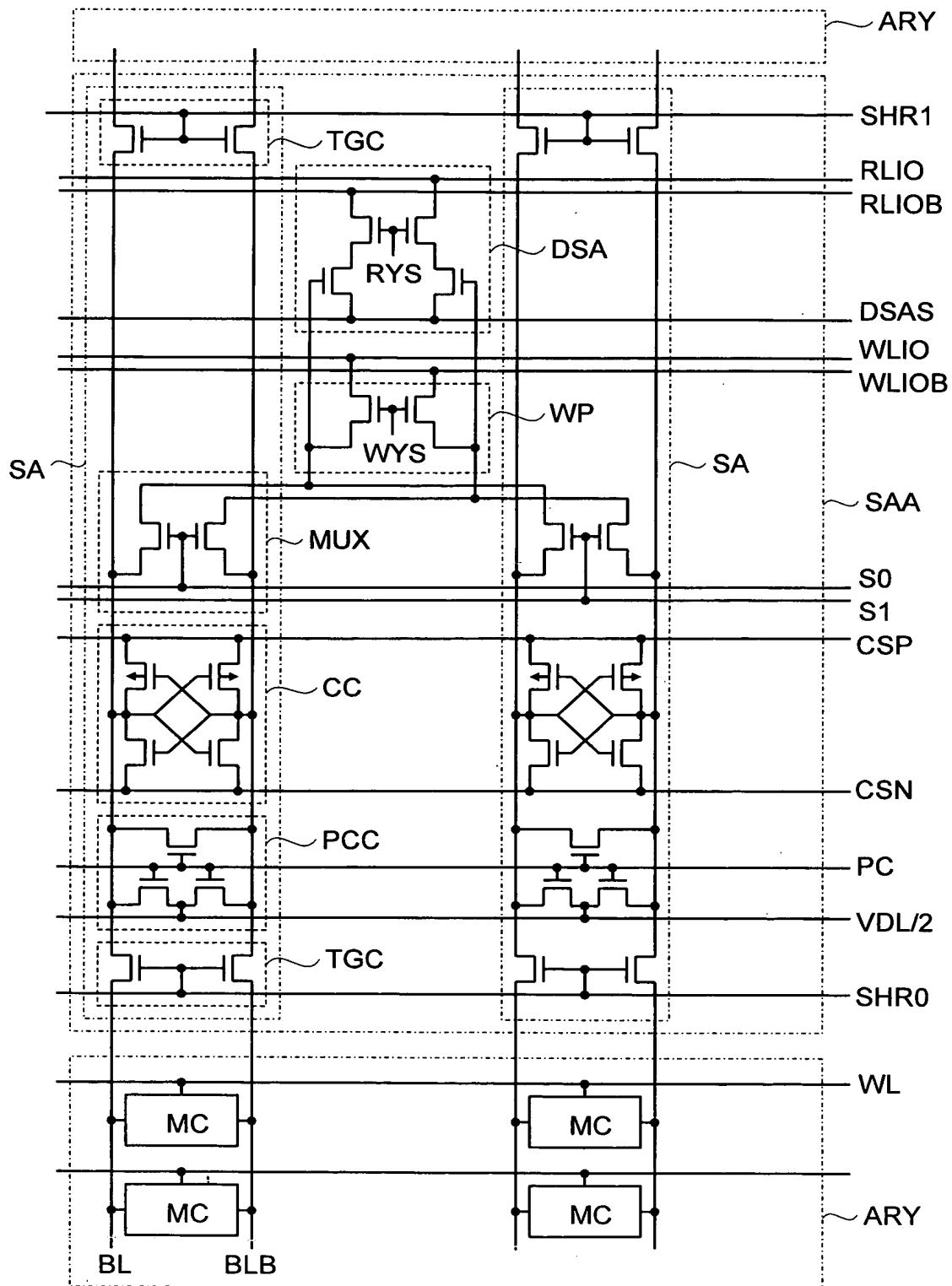
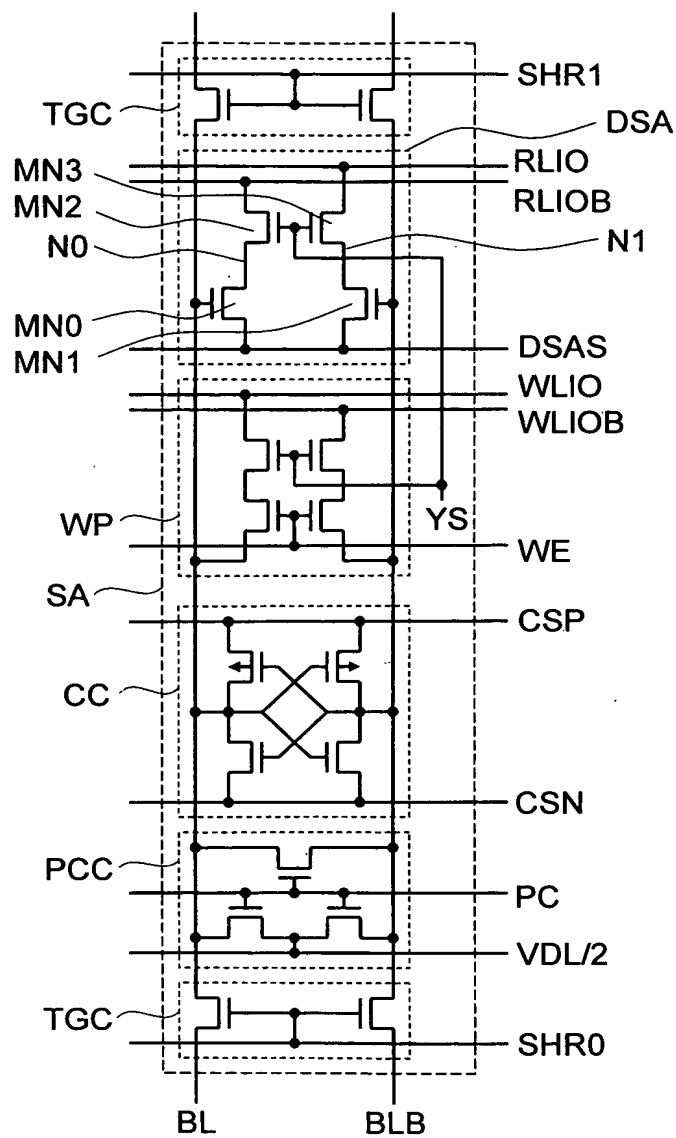
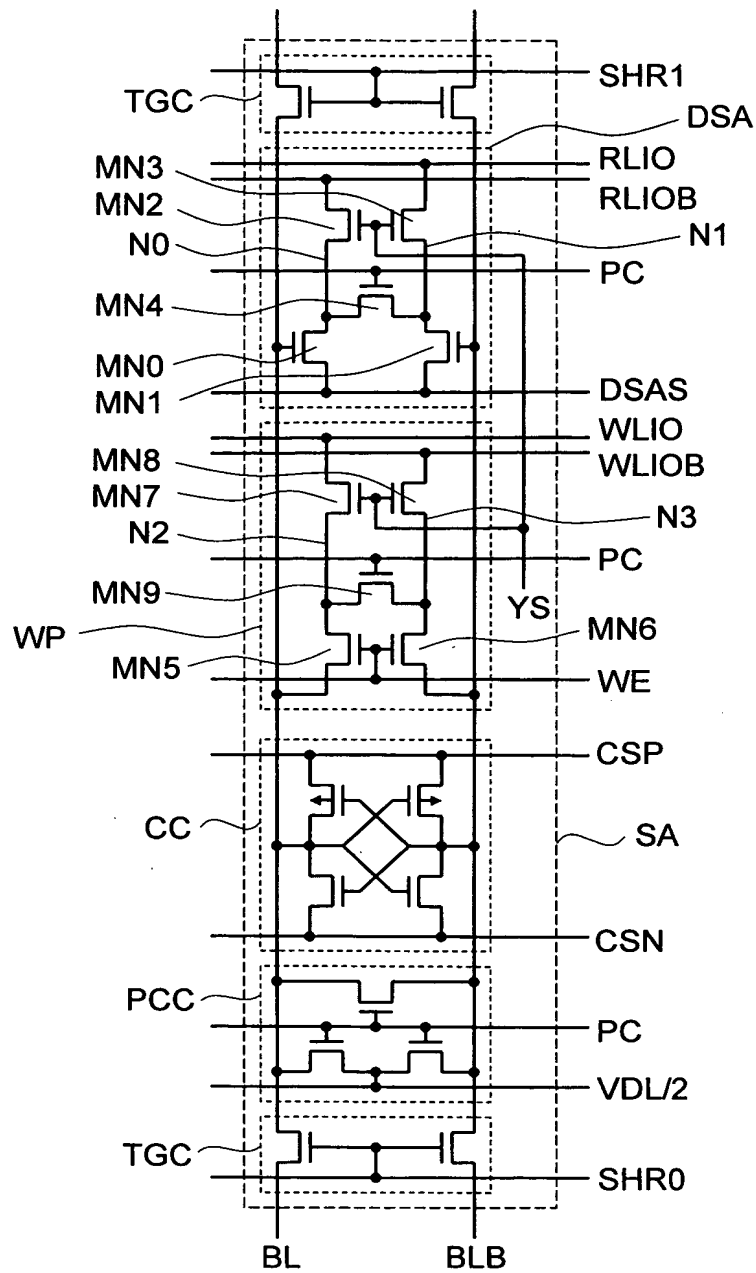


FIG. 14



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FIG. 15



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FIG. 16

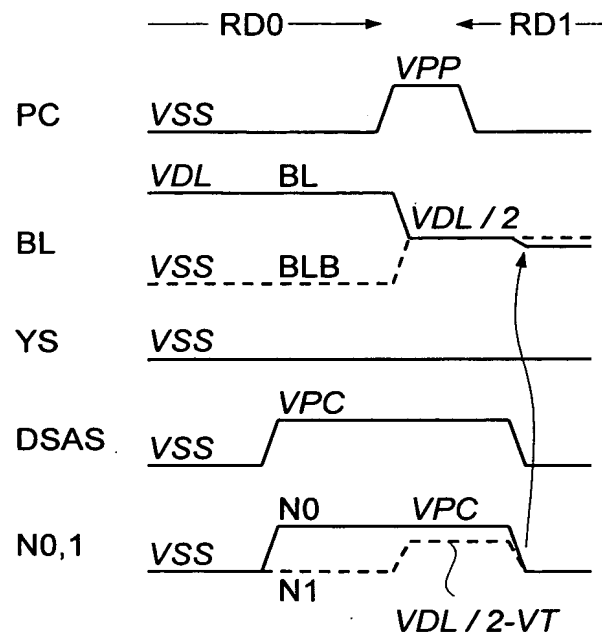
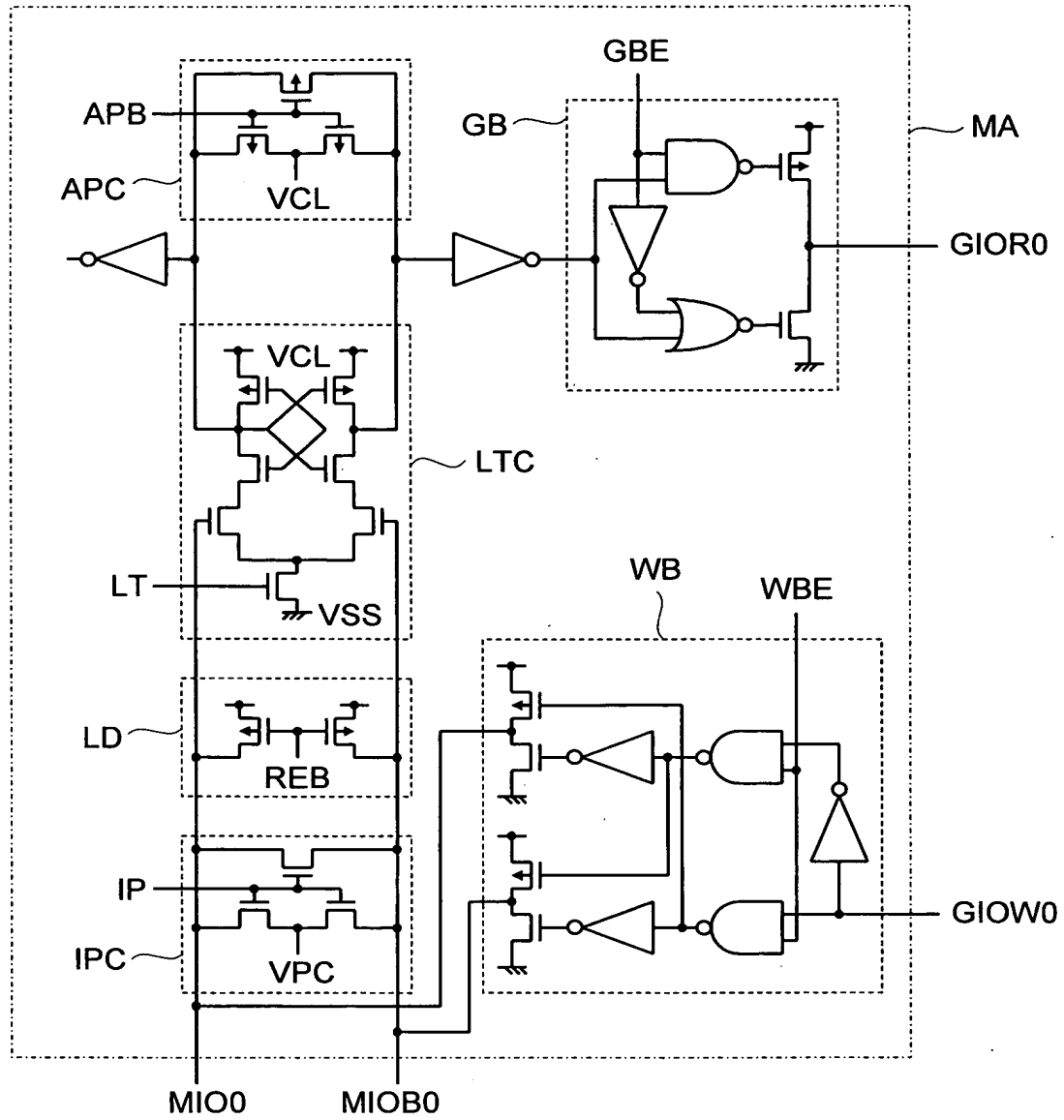


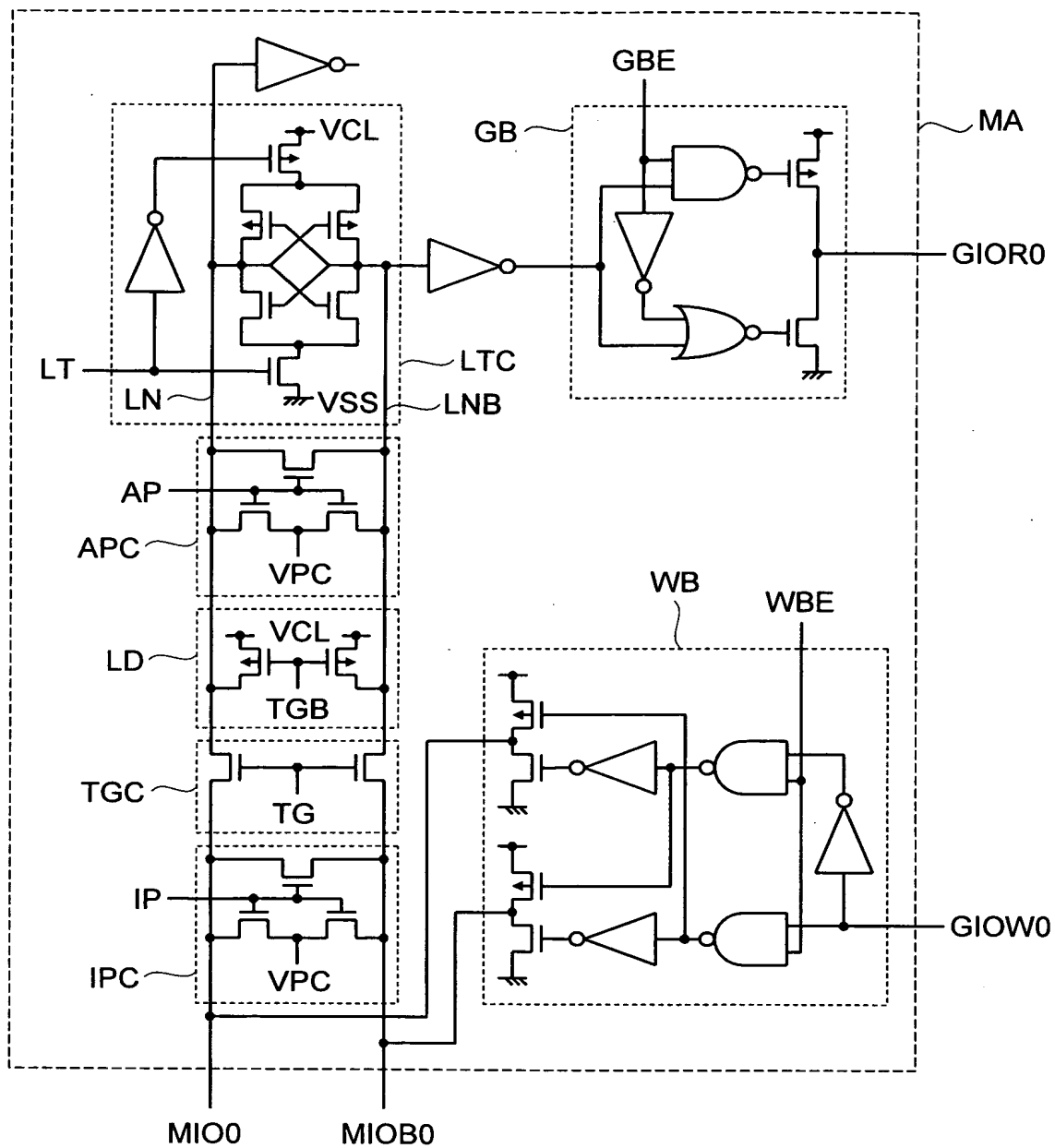


FIG. 17



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FIG. 18



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FIG. 19

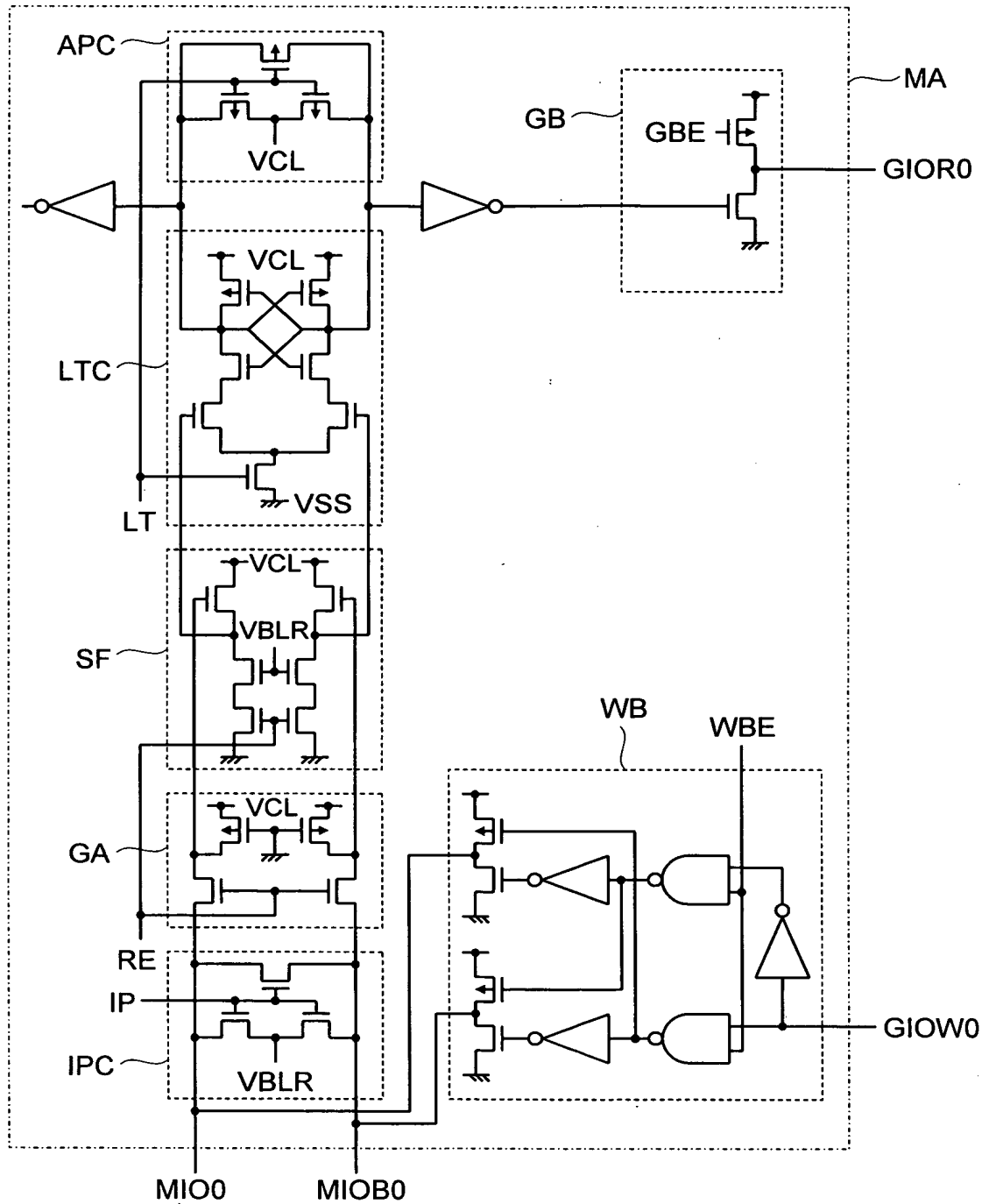
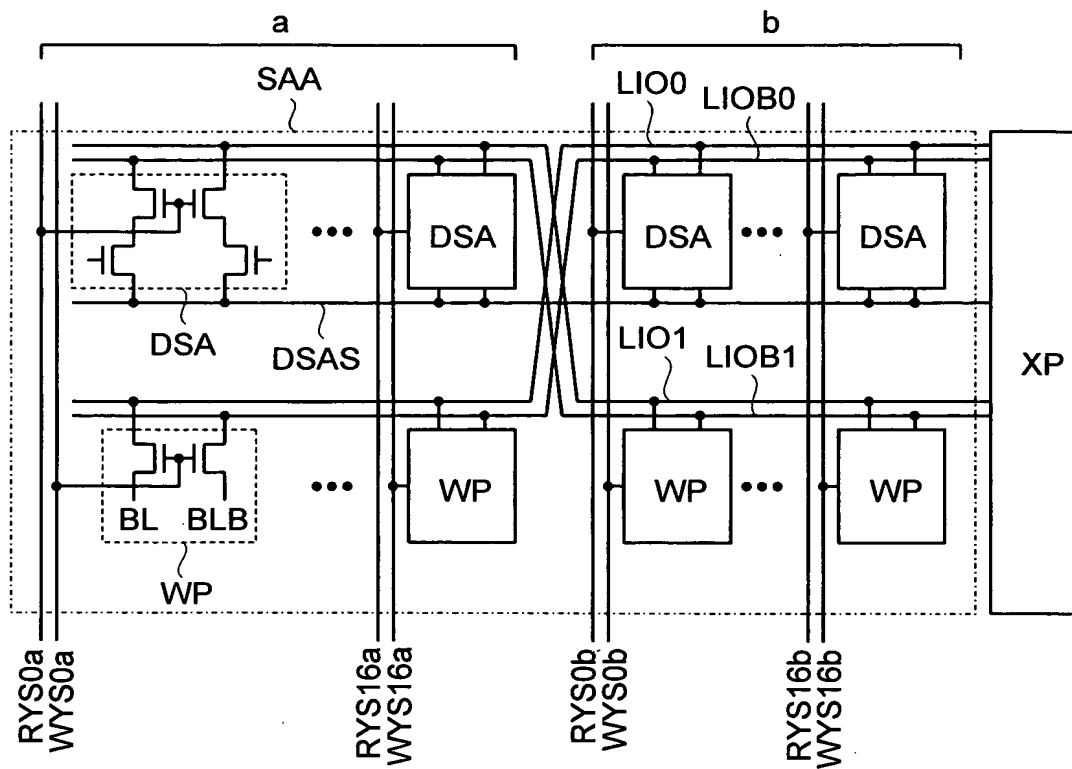


FIG. 20



The diagram illustrates a semiconductor device architecture. On the left, a memory array (ARY) is shown with a word line (WL) and bit lines (BL, BLB) connected to a memory cell (MC). The array is controlled by a sense amplifier (SA) and a data storage amplifier (DSA). The right side of the diagram shows a peripheral logic block (XP) containing various control and data paths, including RGC, BA, CP, GT, RE, LD, LPC, and VPC, connected to MIOB and MIO lines.

FIG. 22

